

C3 26. [Amended] The method of claim [25,] 21 wherein  $x$  is selected such that the transistor has a [the desired] charge retention time [is approximately] of between 1 second and  $10^6$  years.

C4 32. [Twice Amended] The method of claim 29, further comprising oxidizing the gate [material] to form a thin layer of oxide on the gate [material].

C5 43. [Amended] A method of fabricating a transistor comprising:  
forming an insulating layer on a substrate;  
forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0; and  
removing portions of the insulating layer and the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  to form a gate on the substrate.

C6 45. [Amended] The method of claim 43, further comprising:  
[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]  
forming a well region in the substrate;  
forming field oxide on the substrate to define an active region;  
doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer; and  
wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;  
wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer; and  
wherein removing comprises:  
patterning the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ ; and  
etching the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

C1  
50. [Amended] A method of fabricating a transistor comprising:  
forming an insulating layer on a silicon substrate;  
forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is  
between 0 and 1.0;  
doping the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  with a p-type implantation; and  
removing portions of the insulating layer and the layer of the silicon carbide compound  
 $\text{Si}_{1-x}\text{C}_x$  to form a gate on the substrate.

C8  
52. [Amended] The method of claim 50, further comprising:  
[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon  
carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]  
forming a well region in the silicon substrate;  
forming field oxide on the silicon substrate to define an active region;  
doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide  
compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer; and  
wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of  
tunnel oxide on a silicon substrate by dry thermal oxidation;  
doping the layer comprises doping the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  with  
a p-type implantation of a boron dopant;  
wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a  
film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the  
insulating layer; and  
wherein removing comprises:  
patterning the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ ; and  
etching the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer  
to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching  
and reactive ion etching.

C9  
55. [Amended] A method of fabricating a transistor comprising:  
forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0;

doping the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  with an n-type ion implantation;

and

removing portions of the insulating layer and the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  to form a gate on the substrate.

57. [Amended] The method of claim 55, further comprising:

[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ ; and

etching the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

60. [Amended] A method of fabricating a floating gate transistor comprising:

forming an insulating layer on a substrate;

forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound

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Si<sub>1-x</sub>C<sub>x</sub> to form a floating gate on the substrate;  
forming an intergate dielectric on the floating gate; and  
forming a control gate over the intergate dielectric.

*CH*

62. [Amended] The method of claim 60, further comprising:  
[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> and the insulating layer;]  
forming a well region in the substrate;  
forming field oxide on the substrate to define an active region;  
doping the silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> while forming the layer of the silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> on the insulating layer;  
forming a source region and a drain region in the substrate and separated by a channel region in the substrate; and  
wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;  
wherein forming a layer of a silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> comprises depositing a  
*sub*  
*D8* film of a polycrystalline or microcrystalline doped silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> on the insulating layer;  
wherein removing comprises:  
patterning the layer of the silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub>; and  
etching the layer of the silicon carbide compound Si<sub>1-x</sub>C<sub>x</sub> and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;  
wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and  
wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

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65. [Amended] A method of fabricating a floating gate transistor comprising:  
forming an insulating layer on a silicon substrate;

forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0;

doping the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound

$\text{Si}_{1-x}\text{C}_x$  to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

67. [Amended] The method of claim 65, further comprising:

[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;

forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;

wherein removing comprises:

    patterning the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ ; and

    etching the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

    wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

    wherein forming a control gate comprises forming a polysilicon control gate over the

intergate dielectric.

68. [Amended] A method of fabricating a memory cell comprising:
- forming an insulating layer on a substrate;
  - forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0;
  - removing portions of the insulating layer and the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  to form a floating gate on the substrate;
  - forming an intergate dielectric on the floating gate; and
  - forming a control gate over the intergate dielectric.

70. [Amended] The method of claim 68, further comprising:
- [selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]
  - forming a well region in the substrate;
  - forming field oxide on the substrate to define an active region;
  - doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;
  - forming a source region and a drain region in the substrate and separated by a channel region in the substrate; and
  - wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;
  - wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;
  - wherein removing comprises:
    - patterning the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ ; and
    - etching the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

73. [Amended] A method of fabricating a memory cell comprising:  
forming an insulating layer on a silicon substrate;  
forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein  $x$  is between 0 and 1.0;  
doping the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  with an n-type ion implantation;  
removing portions of the insulating layer and the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  to form a floating gate on the silicon substrate;  
forming an intergate dielectric on the floating gate; and  
forming a control gate over the intergate dielectric.

75. [Amended] The method of claim 73, further comprising:  
[selecting  $x$  to establish an approximate barrier energy between the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  and the insulating layer;]  
forming a well region in the silicon substrate;  
forming field oxide on the silicon substrate to define an active region;  
doping the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  while forming the layer of the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;  
forming a source region and a drain region in the silicon substrate and separated by a channel region in the silicon substrate; and  
wherein forming an insulating layer comprises forming a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;  
wherein forming a layer of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer;  
wherein removing comprises: